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MPEG-4 PART 10/HEVC DCT ARCHITECTURE EFFICIENT INTEGER

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ABSTRACT

In this project we have proposed a low-cost high throughput multistandard transform (MST) core, which can support MPEG 1/2/4 (8 × 8), H.264 (8 × 8 &4 × 4), and Video Codecs VC-1 (8 × 8, 8 × 4, 4×8 & 4×4) transforms. Common sharing distributed arithmetic (CSDA) algorithm combines factor sharing and distributed arithmetic sharing techniques, to exploit the available resources on FPGAs, which incorporates pipelining and parallel processing of the input samples. With the help of this architecture the throughput of the design is increased. The main strategy is to reduce the nonzero elements using CSDA algorithm. The reduction in adders in the proposed MST is achieved up to 44.5%, compared with the direct implementation method. The proposed MST core has an eightfold operation frequency throughput rate with eight parallel computation paths

KEYWORDS: Common sharing distributed arithmetic (CSDA),discretecosine transforms (DCT), FPGA, Multistandard transform (MST)

I. INTRODUCTION

Different transforms are widely used in image and video compression applications. Various groups, such as The International Organization for Standardization (ISO), International Telecommunication Union Telecommunication Standardization Sector (ITU-T), and Microsoft Corporation, have developed different Transform dimensions and coefficients, corresponding to several applications.

Discrete Cosine Transform represents the finite sequences of data points in terms of sum of cosine term functions oscillating at different frequencies. 2D DCT is often used in signal and image processing because of its strong energy compaction property.

Number of researchers have worked on various transform core designs, that includes discrete cosine transform (DCT) as well as integer transform, which uses distributed arithmetic(DA), factor sharing (FS) , and matrix decomposition methods for reducing hardware cost. The inner product can be implemented using ROMs and accumulators at place of multipliers that reduces the area cost. Yu and Swartzlander present very efficient method for reducing size of ROMs with recursive DCT algorithms. Delta matrix is used to share hardware resources using the FS method. They generates matrices for multi standards as linear combinations obtained from the same matrix and delta matrix, and show that by factorization the same matrix coefficients can share the same hardware resources.

Recently, reconfigurable architectures have been proposed as a solution that achieves very good flexibility of processors in field-programmable gate array (FPGA) platform or application-specific integrated circuit (ASIC).

II. LITERATURE REVIEW

1. High-Throughput Multi standard Transform Core Supporting MPEG/H.264/VC-1 Using Common Sharing Distributed Arithmetic ,2014.

Yuan-Ho Chen, Jyun-Neng Chen, Tsin-Yuan Chang, and Chih-Wen Lu.
Researchers have worked on transform core designs, including discrete cosine transform (DCT) and integer transform, using distributed arithmetic (DA), factor sharing (FS) and matrix decomposition methods to reduce hardware cost.

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2. A low-power high-performance DCT architecture,2006.

A. M. Shams, Peng C et al., 2007; Huang C Y et al., 2008; Chen Y H et al., 2011; Chen Y H et. NEDA
In this paper the researchers have employed a bit-level sharing scheme to construct the adder-based butterfly matrix, called new DA (NEDA). To improve the throughput rate of the NEDA method, high throughput adder trees are introduced .

3. Design of area-efficient unified transform circuit for multi-standard video decoder.

H. Chang, S. Kim, S. Lee, and K. Cho.,
This paper proposes use of delta matrix to share hardware resources using the FS method. They derive matrices for multi standards as linear combinations from the same matrix and delta matrix, and show that the coefficients in the same matrix can share the same hardware resources by factorization. Matrices for VC-1 transformation can be decomposed into several small matrices, a number of which are identical for different points transforms. Hardware resources can be shared.

4. An architecture and programming model for a resource efficient coarse grained reconfigurable processor.

S. R. Chalamalasetti, S. Purohit, M.Margala, and W. Vanderbauwhede,

This paper proposes the recently reconfigurable architectures have been presented as a solution to achieve a good flexibility of processors in field programmable gate array (FPGA) platform or application-specific integrated circuit (ASIC), such as AP, Ambric, MORA, and Smart Cell. Although these reconfigurable architectures have the feature of flexibility, the pure ASIC design can be recommended for a fixed customer application suitably.

III. MATERIALS AND METHODS

The proposed CSDA combines the FS and DA methods to gain better resource sharing for inner-product operation. The FS and DA method are described in the following.

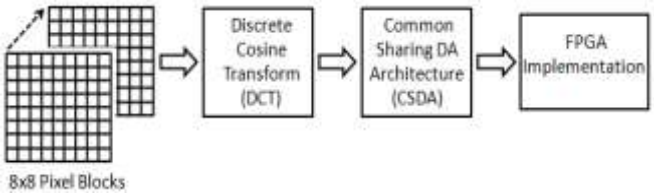

Fig 1 Block diagram

1. Mathematical Derivation of Factor Sharing

In Factor Sharing method the same factor is shared in different coefficients among the same input. Consider two different elements *S*1 and *S*2 having the same input *X* as an example

$$S1 = C1X,\ S2 = C2X. \qquad (1)$$

Assuming that thecoefficients *C*1 and *C*2 having same factor *Fs* can be found in the, (1) can be rewritten as follows:

$$S1 = (Fs2k1 + Fd1)X$$
$$S2 = (Fs2k2 + Fd2)X \qquad (2)$$

where*k*1 and *k*2 specifies the weight position of the sharedfactor *Fs* in coefficientsC_1 and C_2, respectively. Theremainder coefficients are *Fd*1 and *Fd*2 after extracting the shared factor *Fs* forcoefficients C_1 and C_2, respectively

$$Fd1 = C1 - Fs2k1$$

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Fd2= C2− Fs2k2. *(3)*

2. Mathematical Derivation of CSD Format Distributed

Arithmetic

For a general matrix multiplication-and accumulation the inner product can be written as follows:

$$Y = \mathbf{A}^T\mathbf{X} = \sum_{i=1}^{L} A_i X_i \qquad (4)$$

whereAi is an N-bit CSD coefficient, and the inputdata is Xi. Equation (4) can be given as listed below

$$Y = \begin{bmatrix} 2^0 & 2^{-1} & \cdots & 2^{-(N-1)} \end{bmatrix} \cdot \begin{bmatrix} A_{1,0} & A_{2,0} & \cdots & A_{L,0} \\ A_{1,1} & A_{2,1} & \cdots & A_{L,1} \\ \vdots & \vdots & \ddots & \vdots \\ A_{1,(N-1)} & A_{2,(N-1)} & \cdots & A_{L,(N-1)} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ \vdots \\ X_L \end{bmatrix}$$
$$= \begin{bmatrix} 2^0 & 2^{-1} & \cdots & 2^{-(N-1)} \end{bmatrix} \begin{bmatrix} Y_0 \\ Y_1 \\ \vdots \\ Y_{(N-1)} \end{bmatrix} \qquad (5)$$

where$Yj= \sum^{L}A_{i,j} X_i$, $A_{i,j}\in \{-1, 0, 1\}$, and $j= 0, . .(N − 1)$.

In (5), $Y_j$can be computed by addingor subtracting X_i with $A_{i,j}\neq 0$. The resultant product Y can thenbe obtained by shifting and adding every nonzero Y_j. Inthis manner, the inner product computation in (4) and can beimplemented using shifters and adders instead of multipliers.Therefore, CSD DA-based architecture can achieve a efficientarea optimization.

3. Proposed Common Sharing Distributed Arithmetic (CSDA) Algorithm

The proposed CSDA algorithm combines the Factor Sharing (FS) and Distributed Arithmetic (DA)methods. The coefficients matrix is expanded at the bit level thenin each coefficientthe same factors are shared bythe FS method; after thatthe DA method is applied to share the same input combination for each coefficient position.The proposed CSDA algorithm example in a matrix inner product is given asfollows:

$$\begin{bmatrix} Y_1 \\ Y_2 \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} \qquad (6)$$

Where$C11$ and$C22$ are the coefficients of five-bit CSD numbers

$$C_{11} = \begin{bmatrix} 1 & -1 & 1 & 0 & 0 \end{bmatrix}$$
$$C_{12} = \begin{bmatrix} 1 & -1 & 0 & 0 & 1 \end{bmatrix}$$
$$C_{21} = \begin{bmatrix} 1 & 1 & -1 & 0 & 0 \end{bmatrix}$$
$$C_{22} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \end{bmatrix}. \qquad (7)$$

Fig. 1 shows the flow of proposed CSDA algorithm. In these four coefficients the same shared factor Fs is [1 −1], and$C11 \approx C22$ can use Fs instead of [1 −1], with the correspondingposition under the FS method. To share the

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same position for the input,and the DA shared coefficient DA_1which is equal to $(X_1+ X_2)$ *Fs*the DA method is subsequently applied.Finally, the matrix inner products in (6) can be implementedby shifting and adding every nonzero weight position.Fig. 2 shows the coefficient searching flow of the proposedCSDA algorithm. To obtain better resource sharing for inner product operation, the proposed CSDA combines the Factor Sharing andDistributed Arithmetic methods. The FS method is adopted first to findthe factors that have higher hardwareresource sharing capability, where the hardware resource in this paper isdefined as the use of number of adders. Next, the DA methodis used to search the shared coefficient based on the resultsof the Factor Sharing method. The adder-tree circuits will be followedby the designed CSDA circuit. Thus, the CSDA methodaims to reduce the nonzero elements. For estimating the number of adders in the CSDA loop the CSDA shared coefficient is used.Therefore, the iteration searching loop requires a large numberof iteration loops to determine the smallest hardware resource with the help of thesesteps, and the CSDA shared coefficient can be generated.Notice that the optimal factor or coefficient in only FS orDA methods is not conducted for the smallest resource in theproposed CSDA method. Thus, a number of iteration loops areneeded for determining the better CSDA shared coefficient. Anexample of the performance in FS, DA, and CSDA methodsis shown in a later section.Although the joint DA and sub-expression sharing method,which adopts DA method first for eliminating multipliers andthen to reduce the number of adders by the sub-expressionsharing method for sharing the same adder operations, ispresented in, the proposed CSDA method adopts theFS method first to share the same adder operations and thenadopts the DA method to reduce the nonzero term, which canreduce the operation of the adder tree. Therefore, the proposedCSDA improves the sharing capacity and is further adoptedto implement multiple block sizes and coefficients.

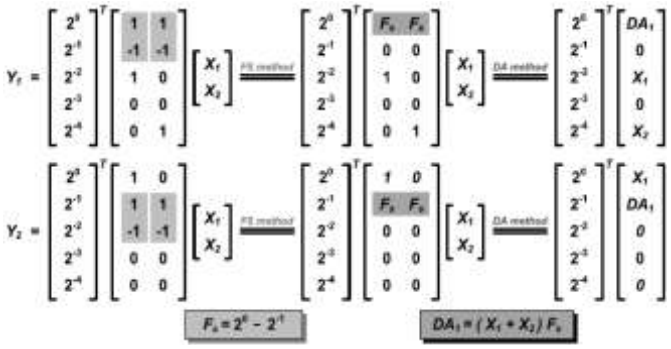

Fig 2 Example of a CSDA algorithm

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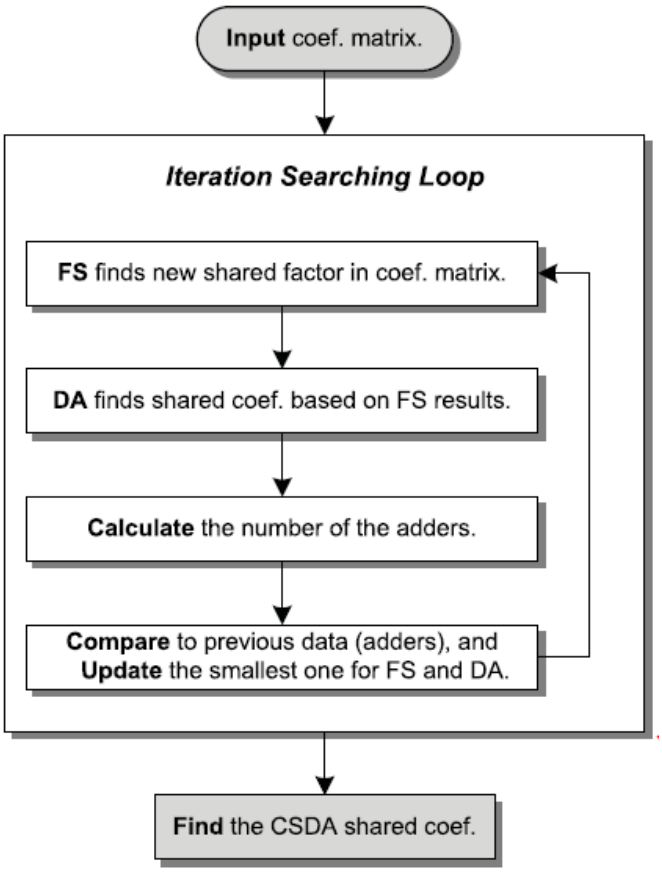

Fig.3 Architecture of the proposed 1-D CSDA-MST

The 1-D eight-point MST corearchitecture is shown in Fig. 3, which consists of a selected butterfly (SBF) module, an even part CSDA (CSDA_E) and an odd part CSDA (CSDA_O), eight error-compensated error trees (ECATs) and a permutation module.

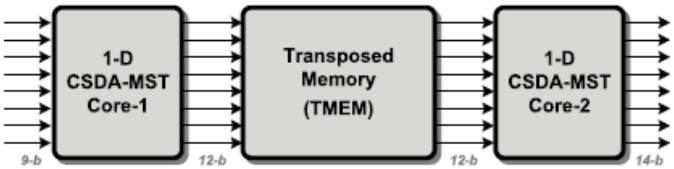

Fig4 Architecture of the proposed 1-D CSDA-MST

The designed 2-D CSDA-MST core consists of two 1-D CSDA-MST core with Core-1 and Core-2 having a transposed memory (TMEM), as shown in Fig. 4. Core-1 and Core-2 have different word length for each arithmetic, register, and MUX. The TMEM is designed using sixty-four 12-bit registers, where the output data from Core-1 is transposed and fed into Core-2. Both coreshave four pipeline stages: two in the even and odd part CSDA circuit, and two in ECATs. Therefore, the proposed 2-D CSDA-MST core has a latency of 16 clock cycles (= 4 + 8 + 4), and the TMEM executes transposed operation after 12 clock cycles (= 4 + 8) when 8 pixels are input.

IV. RESULTS AND DISCUSSION

In this paper we have proposed a MST core that supports MPEG-1/2/4 (8 × 8), H.264 (8 × 8 &4 × 4), and Video CodesVC-1 (8 × 8, 8 × 4, 4 × 8 & 4 × 4) transforms. However, the proposed MST core includes DA and FS schemes as common sharing distributed arithmetic (CSDA) that reduces the hardware cost. The main strategy is to reduce the nonzero elements using CSDA algorithm; which results in, few requirement of adders in the adder-tree circuit. According to the proposed designed strategy, the selected canonic signed digital (CSD) coefficients can achieve excellent sharing capability for hardware resources.

V. CONCLUSION

The CSDA-MST core can achieve high performance, with a high throughput rate and low-cost VLSI design, supporting MPEG-1/2/4, H.264, and VC-1 MSTs. By using the proposedCSDA method, the number of adders and MUXs in the MST core can be saved efficiently. Measured results show the CSDA-MST core with a throughput rate of 1.28 G-pels/s, which can support (4928 × 2048@24 Hz) digital cinema format with only 30 k logic gates. Because visual media technology has advanced rapidly, this approach will help meet the rising high-resolution specifications and future needs.

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